

FIG. 3

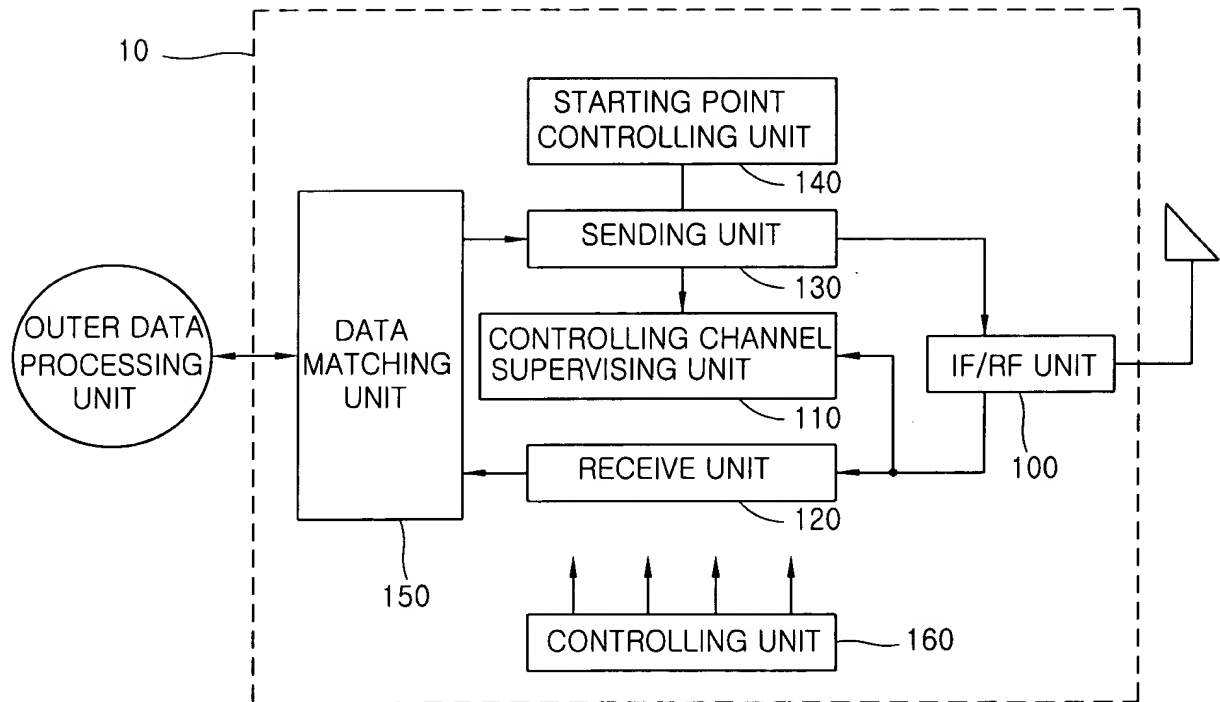
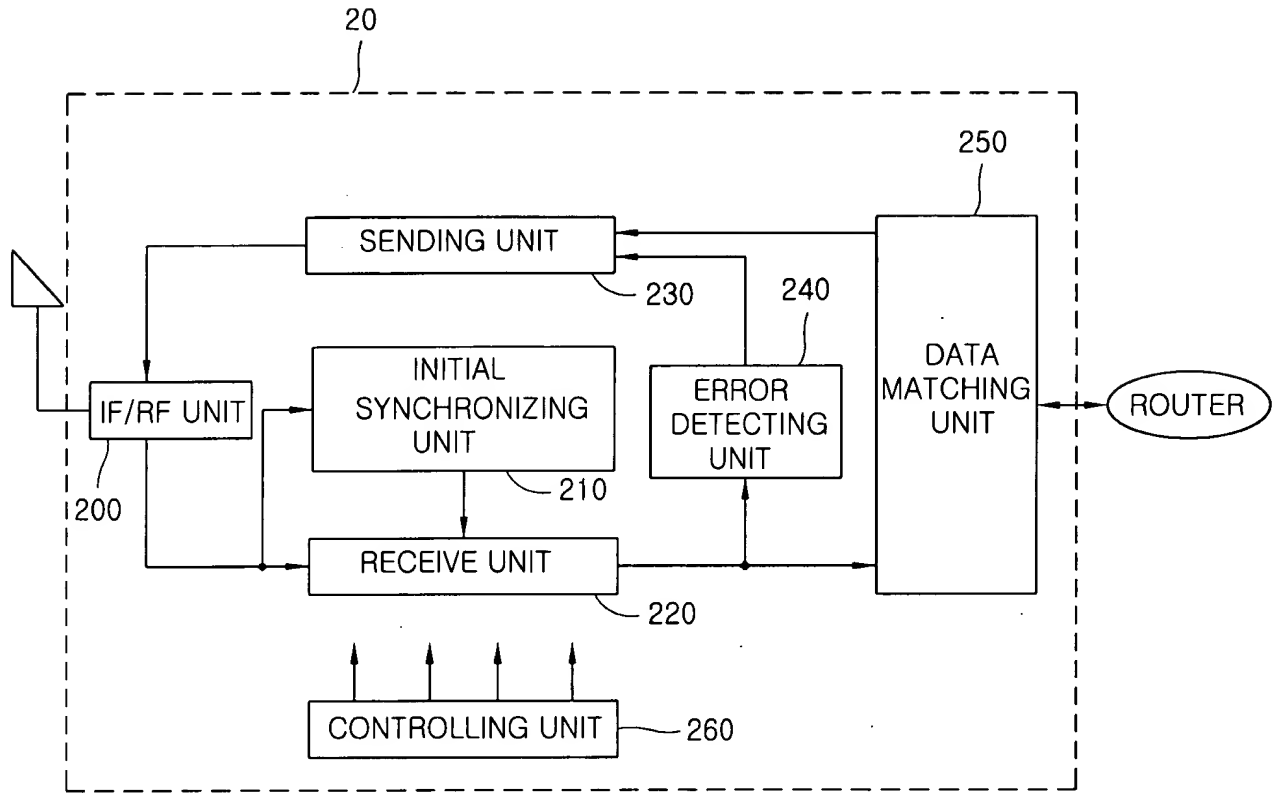


FIG. 3

FIG. 4



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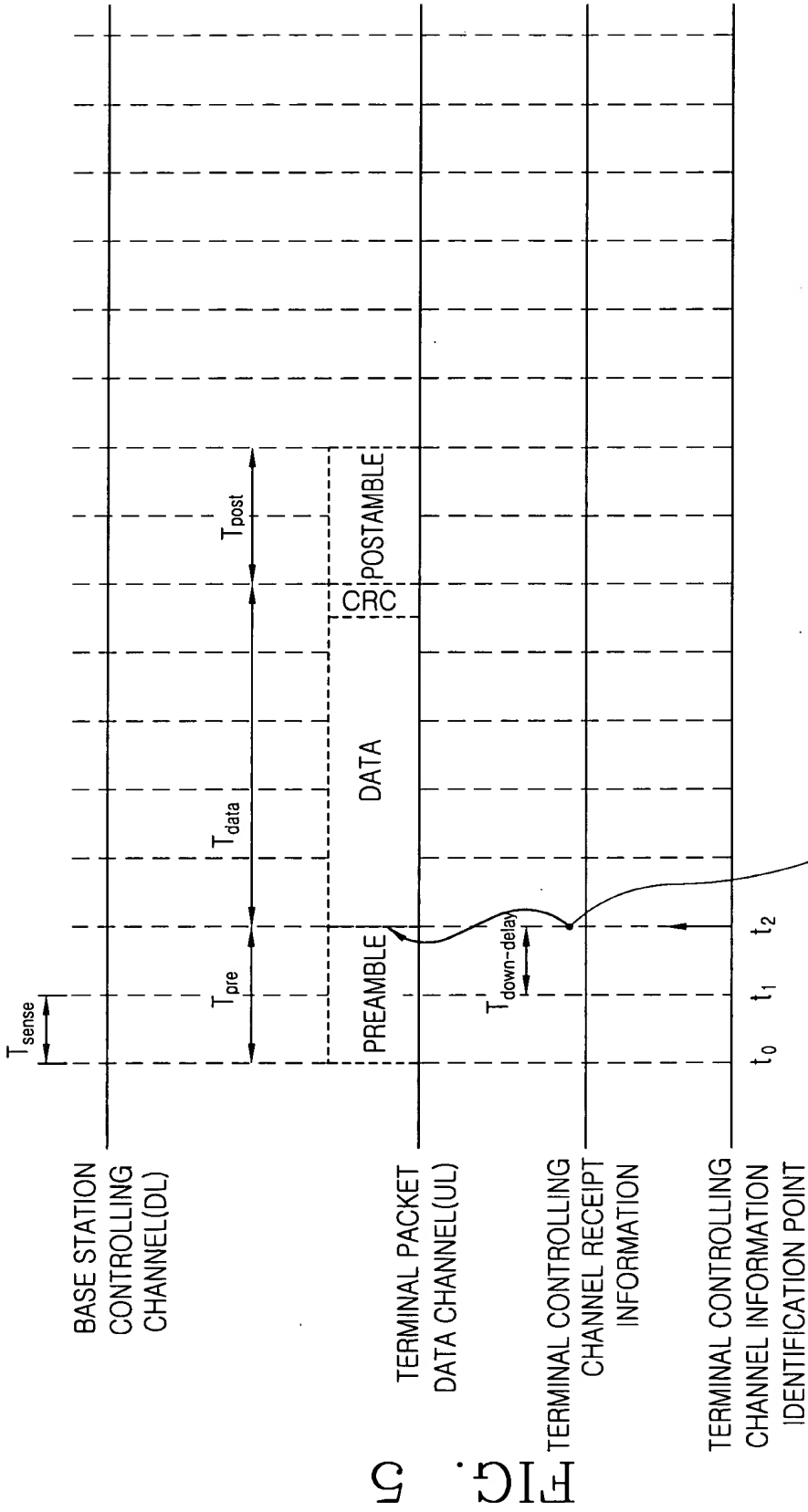


FIG. 5

T_{pre}	:PREAMBLE TIME=4096xN CHIPS
T_{data}	:PACKET DATA TIME=VARIABLE
T_{post}	:POSTAMBLE TIME=2048xM CHIPS
T_{sense}	:BASESTATION ENERGY DETECT TIME
$T_{down-delay}$:DOWNLINK PATH DELAY TIME

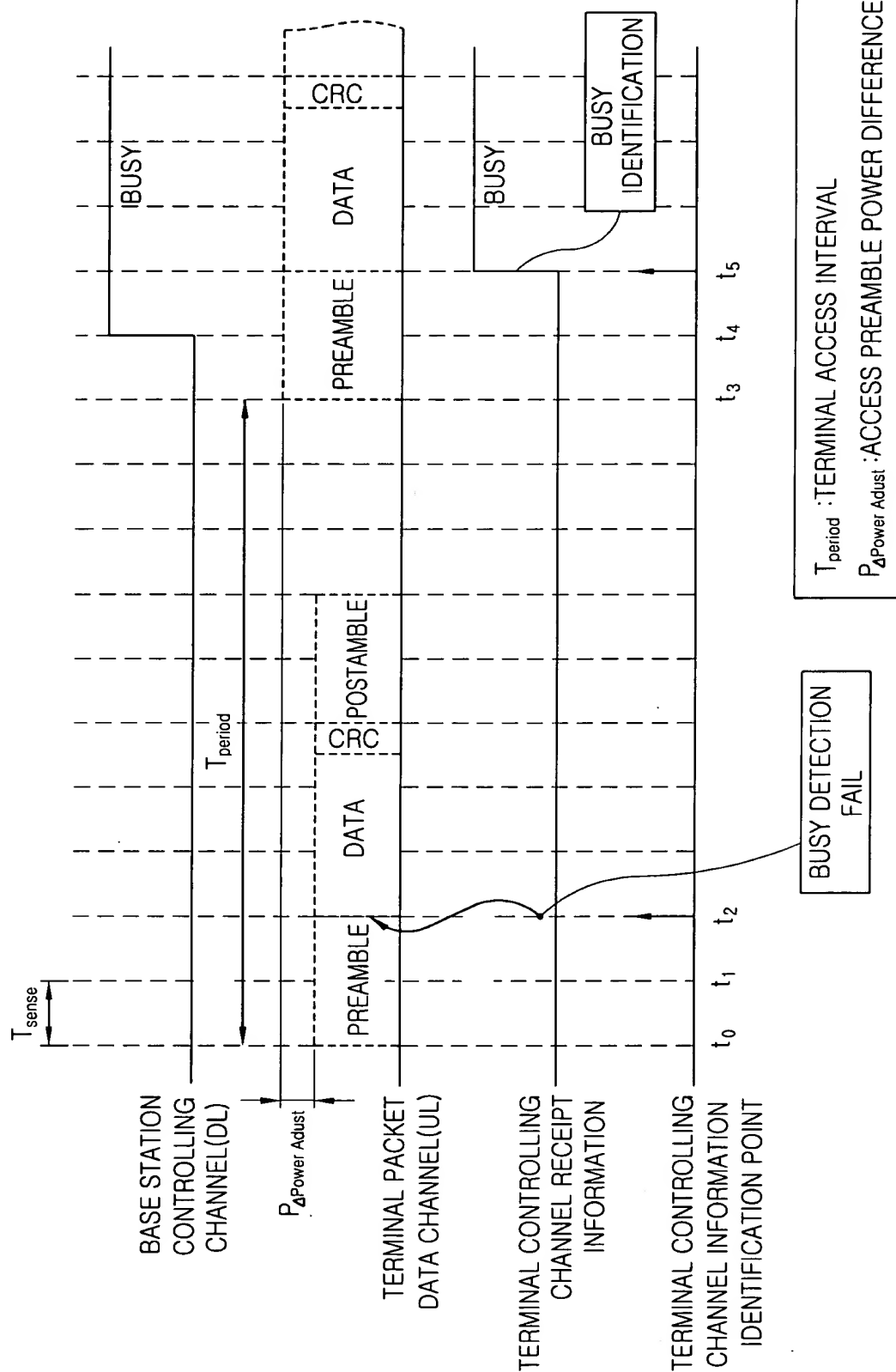
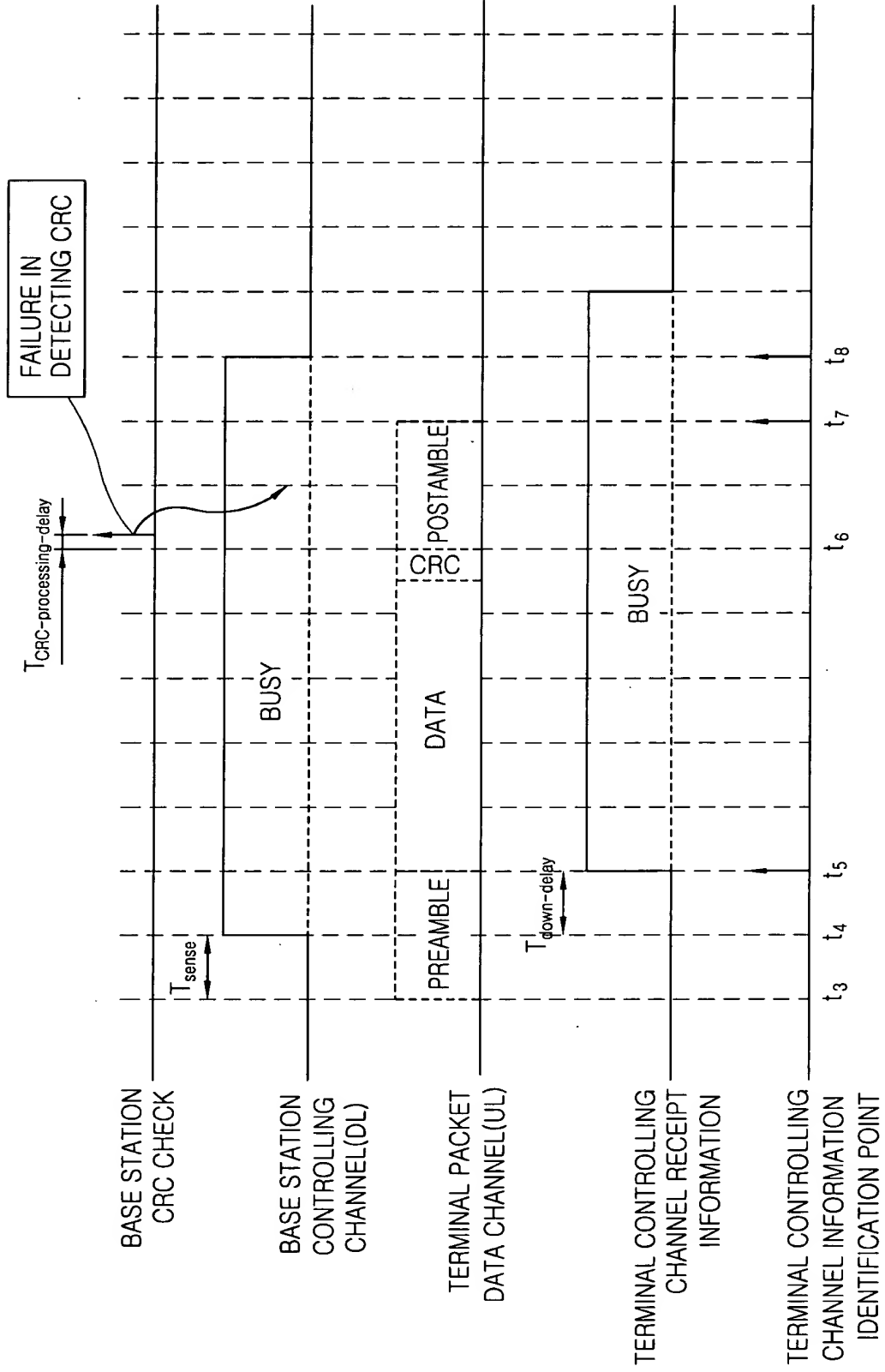


FIG. 2



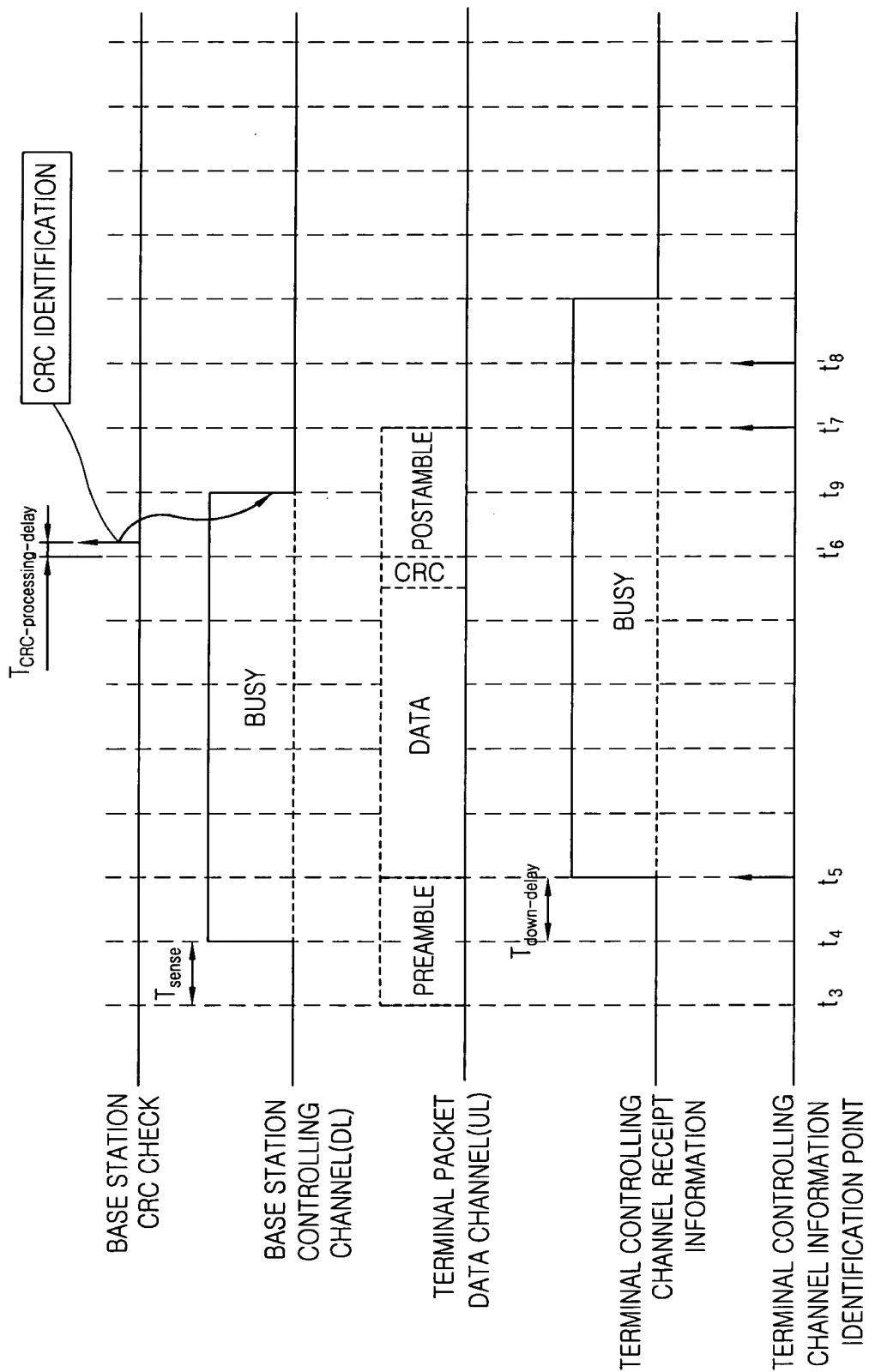


FIG. 8

FIG. 9

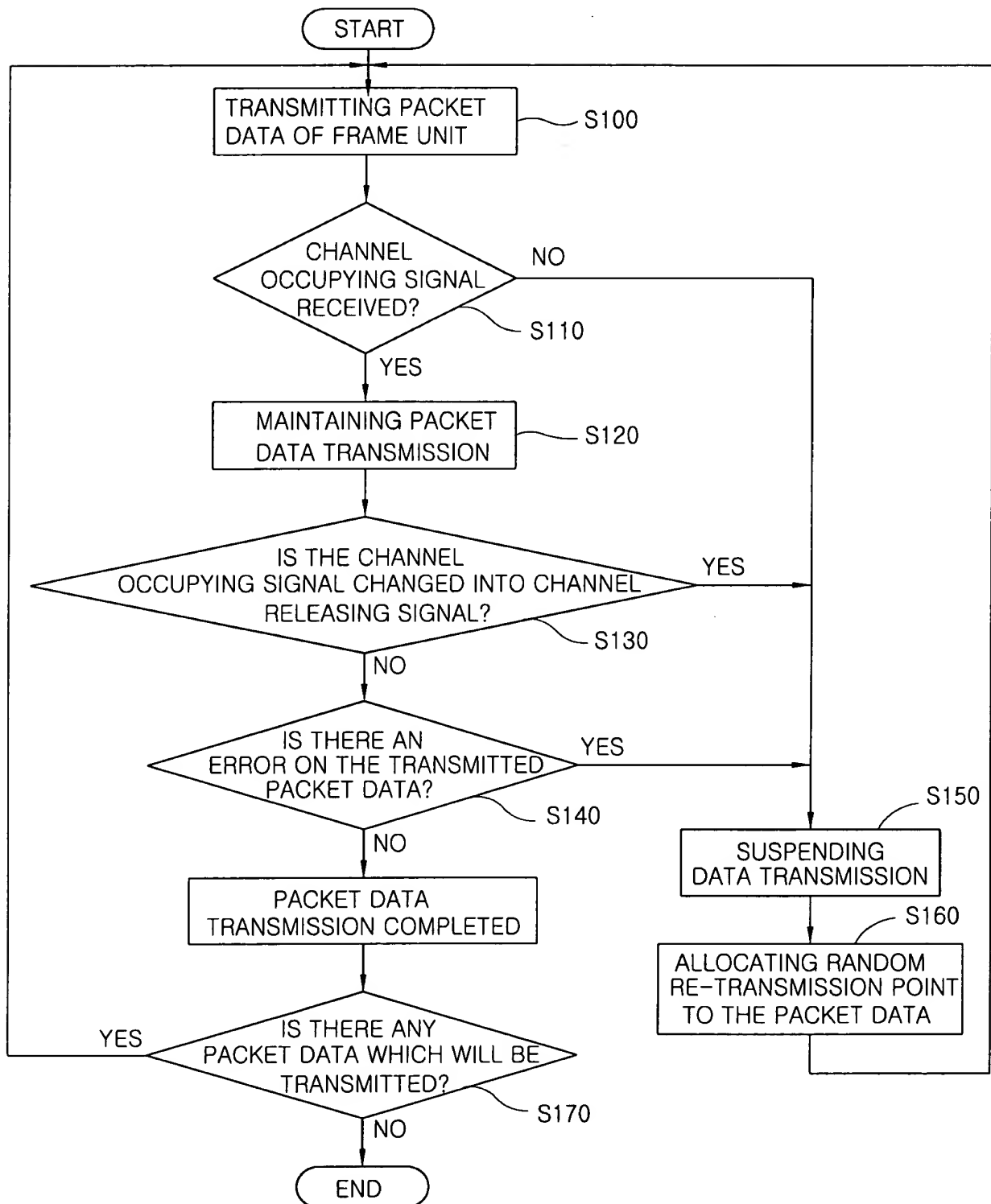


FIG. 9